WHAT IS CLAIMED IS:

1. A method for fabricating a semiconductor device, comprising the steps of:

a) forming an insulating film of a carbon-containing silicon oxide film on a substrate;

b) etching the insulating film using a resist pattern as a mask, thereby forming an interconnect groove in the insulating film;

c) performing a dry etching process, thereby removing a cured layer and forming a silicon oxide layer on the bottom and side faces of the interconnect groove,

d) removing the resist pattern by a wet etching process; and

e) filling the interconnect groove with a metal film to form a metal interconnect.

2. The method of Claim 1, wherein the performing a dry etching process, thereby removing a cured layer and forming a silicon oxide layer on the bottom and side faces of the interconnect groove at the same time.

3. The method of Claim 1, wherein the dry etching process uses an etching gas containing oxygen.

4. The method of Claim 1, wherein the dry etching process is formed within a plasma ambient at a pressure of 13.3 Pa or more.

5. The method of Claim 1, wherein the dry etching process is an anisotropic RIE process.

6. The method of Claim 1, further comprising the steps of removing the silicon oxide layer, existing on the bottom and side faces of the interconnect groove, by a wet etching process.

7. The method of Claim 1, wherein the silicon oxide layer has a thickness of 20 nm or less.

8. The method of Claim 1, wherein the silicon oxide layer has a density of 2.0 g/cm^3 or more.

9. The method of Claim 1, wherein the metal interconnect is made up of a barrier metal layer and a main interconnect layer.

10. The method of Claim 9, wherein the barrier metal is a tantalum nitride and the main interconnect layer is copper.

11. A method for fabricating a semiconductor device, comprising the steps of:

a) forming an insulating film of a carbon-containing silicon oxide film on a substrate;

b) etching the insulating film using a resist pattern as a mask, thereby forming an interconnect groove in the insulating film;

c) filling the interconnect groove with a resist film;

d) performing a dry etching process, thereby removing a part of the resist film, existing over the interconnect groove, and forming a silicon oxide layer on the carbon-containing silicon oxide film,

e) removing the other part of the resist film, still existing inside the interconnect groove by a wet etching,

f) filling the interconnect groove with a metal film to form a metal interconnect.

12. The method of Claim 11, wherein the dry etching process uses an etching gas containing oxygen.

13. The method of Claim 11, wherein the dry etching process is formed within a plasma ambient at a pressure of 13.3 Pa or more.

14. The method of Claim 11, wherein the dry etching process is an anisotropic RIE process.

15. The method of Claim 11, further comprising the steps of removing the silicon oxide layer by a wet etching process.

16. The method of Claim 11, wherein the silicon oxide layer has a thickness of 20 nm or less.

17. The method of Claim 11, wherein the silicon oxide layer has a density of 2.0 g/cm^3 or more.

18. The method of Claim 11, wherein the metal interconnect is made up of a barrier metal layer and a main interconnect layer.

19. The method of Claim 18, wherein the barrier metal is a tantalum nitride and the main interconnect layer is copper.